iFCP65 Readout

Davide Braga, Luigi Gaioni

Version 6 (9/26/16):

- Corrected Chapt.2.1: the SF transistor for analog readout is a pMOS, not an nMOS
- Corrected Fig.1 (swapped Ibias2 and Ibias1) and Table1 entries for Ibias2 and Ibias1)

Version 5 (9/12/16):

- Corrected Fig.4.

Version 4 (8/18/16):

- Corrected decoupling of IBIAS2 in Table 1.

Version 3 (8/4/16):

- Corrected Pins 12, 15, 18 in Table 1.
- Modified requirements and description entries for SF_OUT in Table 1.

Version 2 (7/29/16):

- Added section on Analog Readout and DLL disabling.
- Corrected Fig.1 (PAD list).
- Corrected IBIAS2 biasing in Table 1.

1.1 Chip Layout

The ASIC is 2 x 2 mm^2, with 94 wire bond pads at the periphery (Fig.1), and 16 x 16 central pads connected to the pixel inputs. The orientation of the chip can be determined by looking at the two missing pads on the left hand side of Fig.1. With the same perspective, the pads on the left hand side are pads belonging to the digital domain, while top and right are analog domain. The bottom and part of the right are reserved for a test structure. Table1 includes a description of the pads and respective properties.

2.1 Chip Readout

Charge injection and readout are controlled via three independent serial-in, parallel-out (SIPO) shift registers (SR) (Fig.2):

- **analog readout** (SR_preamp): the chip has 16 independent outputs (one for each row) to read out the pixel preamplifier output via a pMOS source follower (SF). The related SR has therefore 16 cells, and the data pattern should include a single 1 for correct read out. The 16 outputs (SF_OUT<15:0>) also provide the bias current for the source follower.

- **digital readout** (SR_rd): controls which pixel is connected to the pads HIT, ADC<0:3> to readout the discriminator outputs.

- **charge injection** (SR_inj): controls which pixel(s) is connected to the global line for charge injection (INJ_IN).

As described in Fig.2, the last two SRs are 32b long: the first half addresses the columns (SF[15:0]=cols[15:0]) while the second half is connected to the rows (SF[31:16]=rows[15:0]).

To make sure that only one pixel is selected, there should be a single 1 in each of these two sections. While having more than one pixel selected at the same time would corrupt the digital readout, several pixels can be selected at once for charge injection (with the limitation that shadow pixels will also be selected from the combination of rows and cols selections).

2.2 Control Signals

Each of the three SR have independent controls and pads, namely:

- **SRin**: serial input;

- **Clk**: SR clock;

- **RstB**: reset (active low). All cells are reset to 0.

- **enable**: the SR cells outputs are gated by an AND cell controlled by enable signal, so that during the initial loading the pixel matrix can be shielded from the transient activity on the selection lines. At the end of the loading phase, enable can go high and the values in the SR are passed to the matrix.

- **SRout**: serial output (for testing purposes).

2.3 Readout sequence.

Given that the SRs have independent clocks and control signals, they can be loaded in any sequence or even at the same time. In the following examples the sequence is SR_preAmp, SR_inj and SR_rd.

Fig.3 shows such loading sequence. Data at the SRin input are latched in the SR at the rising edge of the Clk.

The frequency at which the circuits are operated shall be determined during testing, as such the timescale is not explicitly stated in the following figures. A good initial value for the Clk period would be 5ns.

After an initial reset pulse (RstB low), data are presented on SRin and clocked at the rising edge of Clk. This should continue until the SR is filled (x16 for SR_preamp, x32 for SR_inj and SR_rd). At the end enable should go high to “load” the values to the selection lines of the pixel matrix.

The position of the cols and rows (cf. Fig.1) in the SRin data stream are specified in Fig.4: the first bit selects col[0], while the last selects row[15].

Finally, Fig.5 presents a simulation of what should be seen at the pads after injection charge in a pixel.

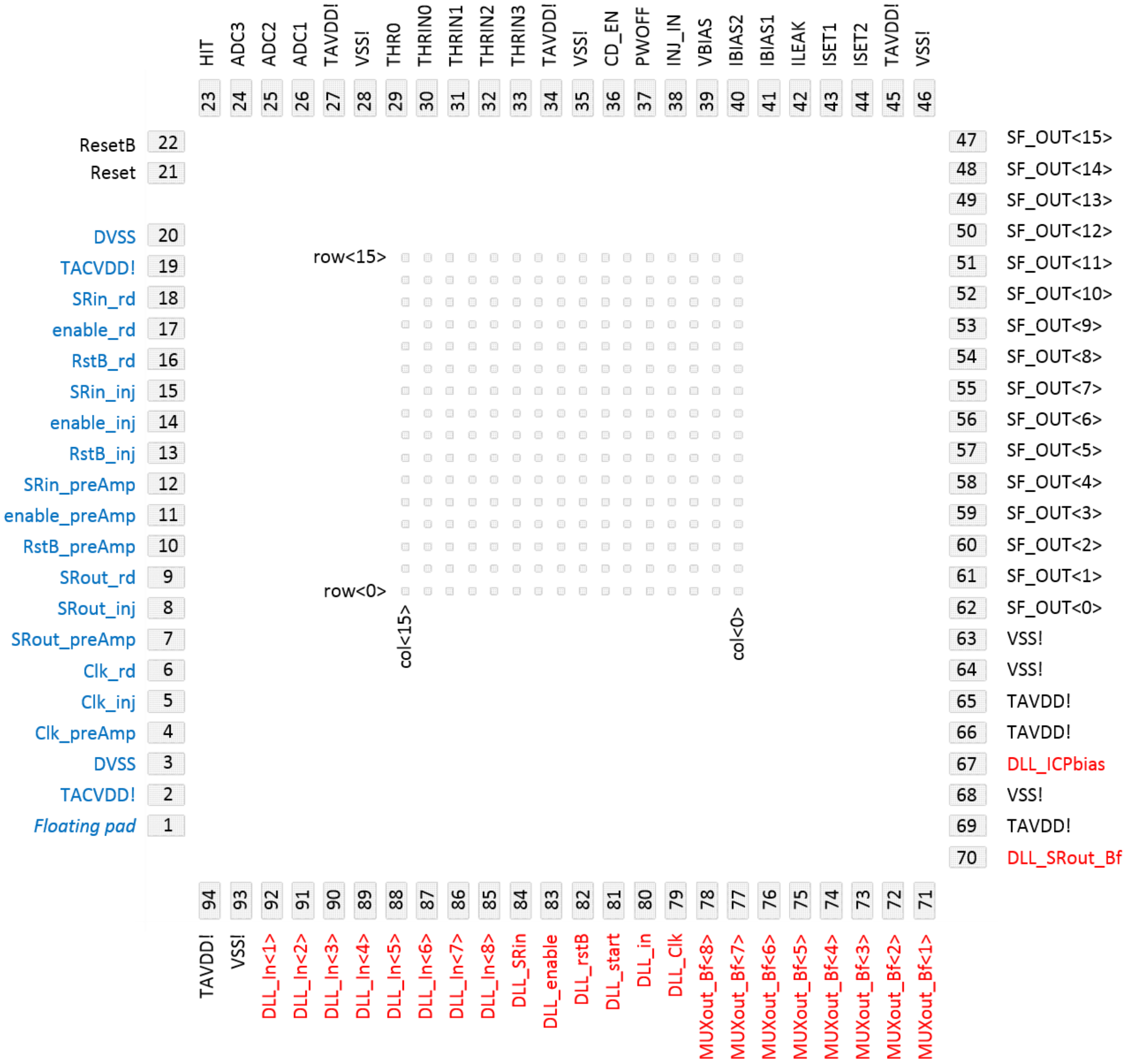

*Figure 1: PAD lists. Blue indicates the **digital** power domain (pads 1 to 20), red the pads specific to the **DLL** test circuit (67 to 94). Red and black both belong to the **analog** power domain. Note two missing pads on the left side.*

Table 1: PAD list

PAD #	PAD name	Type	Typical value	Decoupling	Requirements	Description
1	Floating pad				connect to gnd plane	Floating pad
2, 19	TACVDD!	Digital Power	1.2 V	Decouple to ground plane	<10mA total current drawn	Digital (“core”) VDD
3, 20	DVSS	Digital ground	0 V	Connect externally to ground plane		Digital power supply
4	Clk_preAmp	Digital input	CMOS levels			Shift Register (SR) Clk for the selection of columns for the analog read out.
5	Clk_inj	Digital input	CMOS levels			SR Clk for the selection of pixels for signal injection.
6	Clk_rd	Digital input	CMOS levels			SR Clk for the selection of columns for the digital read out.
7	SRout_preAmp	Digital output	CMOS levels		<10pF load	Serial out for the preamplifier readout SR
8	SRout_inj	Digital output	CMOS levels		<10pF load	Serial out for the injection SR
9	SRout_rd	Digital output	CMOS levels		<10pF load	Serial out for the digital readout SR
10	RstB_preAmp	Digital input	CMOS levels			Reset (active low) for the preamp SR.
11	enable_preAmp	Digital input	CMOS levels			enables preamp SR: content of SR is gated to the pixels (which otherwise see all 0s). Active high.
12	SRin_preAmp	Digital input	CMOS levels			Serial input for the preamp selection.
13	RstB_inj	Digital input	CMOS levels			Reset (active low) for the injection SR.
14	enable_inj	Digital input	CMOS levels			enables injection SR: content of SR is gated to the pixels (which otherwise see all 0s). Active high.
15	SRin_inj	Digital input	CMOS levels			Serial in input for the injection SR.
16	RstB_rd	Digital input	CMOS levels			Reset (active low) for the digital readout SR.
17	enable_rd	Digital input	CMOS levels			enables digital readout SR: content of SR is gated to the pixels (which otherwise see all 0s). Active high.
18	SRin_rd	Digital input	CMOS levels			Serial input for the digital readout SR.
21	Reset	Digital input (analog domain)	CMOS levels			Pixel comparator reset (active high)
22	Reset_B	Digital input (analog domain)	CMOS levels			Pixel comparator resetB
23	HIT	Digital output (analog domain)	CMOS levels			Signals if the pixels has been hit
24	ADC3	Digital output (analog domain)	CMOS levels			
25	ADC2	Digital output (analog domain)	CMOS levels			
26	ADC1	Digital output (analog domain)	CMOS levels			
27, 34,	TAVDD!	Analog Power	1.2 V	Bypass at chip to VSS!/gnd plane		Analog power supply

45, 65, 66, 69, 94						
28, 35, 46, 63, 64, 68, 93	VSS!	Analog ground	0 V	connect to gnd plane		Analog ground. Also ESD reference gnd
29	THR0	Analog bias		decouple to VSS!/gnd plane		Reference threshold
30	THRIN0	Analog bias		decouple to VSS!/gnd plane		Threshold for pixel Comparator 0
31	THRIN1	Analog bias		decouple to VSS!/gnd plane		Threshold for pixel Comparator 1
32	THRIN2	Analog bias		decouple to VSS!/gnd plane		Threshold for pixel Comparator 2
33	THRIN3	Analog bias		decouple to VSS!/gnd plane		Threshold for pixel Comparator 3
36	CD_EN	Digital input (analog domain)	CMOS levels	decouple to VSS!/gnd plane		Connects a capacitance (34.4fF) to the pixel input. Global signals: all the pixels share the same line. Active high
37	PWOFF	Digital input (analog domain)	CMOS levels	decouple to analog VDD		Powers off the comparators 3,2,1 in the pixels
38	INJ_IN	Analog input step function		Should be pulsed		Analog value for injection through pixel inj cap (14.9fF) Negative going pulse
39	VBIAS	Analog bias		Decouple to analog VDD	Extract 140uA, expected voltage 0.56V → 4KOhm resistor to analog ground	Bias for the pixel comparators
40	IBIAS2	Analog Bias		decouple to analog VSS	Inject 20uA, expected voltage = 0.45V → R= 37.5 KOhm resistor to analog VDD	Current bias for the preamp second stage
41	IBIAS1	Analog bias		decouple to analog VDD	Extract 20uA, expected voltage = 0.45V → R= 22.5 KOhm resistor to analog ground	Current bias for the preamp first stage
42	ILEAK	Analog Bias		decouple to analog VDD	Extract 1.5uA, expected voltage = 0.9V	leakage current setting

					→ 600 KOhm resistor to analog ground	
43	ISET1	Analog Bias		decouple to analog VDD	Extract 75uA, expected voltage = 0.55V → R= 7.3 KOhm to analog ground	comparator control voltage (1)
44	ISET2	Analog Bias		decouple to analog VSS/gnd plane	Inject 12.5uA, expected voltage = 0.48V → R = 57.6 KOhm to analog VDD	comparator control voltage (2)
47 … 62	SF_OUT<15:0>	Analog output and source follower bias			Inject 750uA, expected voltage = 0.85 V → R = 5.5 KOhm to 5V	outputs of SF for rows 15:0. The SF needs biasing through a resistor to 5V. This voltage should be ramped on after the chip is biased.
67	DLL_ICPbias	Analog Bias			Inject 5uA, expected voltage = 412mV → R= 158KOhm to DLL VDD	Charge pump bias current
70	DLL_SRout_Bf	Digital output	CMOS levels			Serial out for DLL Shift Register
71 … 78	MUXout_Bf<1:8>	Digital output	CMOS levels			Outputs of the DLL
79	DLL_Clk	Digital input	CMOS levels			Clk for the DLL SR
80	DLL_in	Digital input	CMOS levels			Reference Clk for the DLL
81	DLL_start	Digital input	CMOS levels			Control signal for the DLL PFD circuit. For DLL startup (active high)
82	DLL_rstB	Digital input	CMOS levels			rstB for the DLL SR flip flops
83	DLL_enable	Digital input	CMOS levels			enables DLL SR: content of SR is gated to the DLL MUX (which otherwise see all 0s). Active high.
84	DLL_SRin	Digital input	CMOS levels			Serial In for the DLL SR
85 … 92	DLL_In<8:1>	Digital input	CMOS levels			Input signals to the DLL

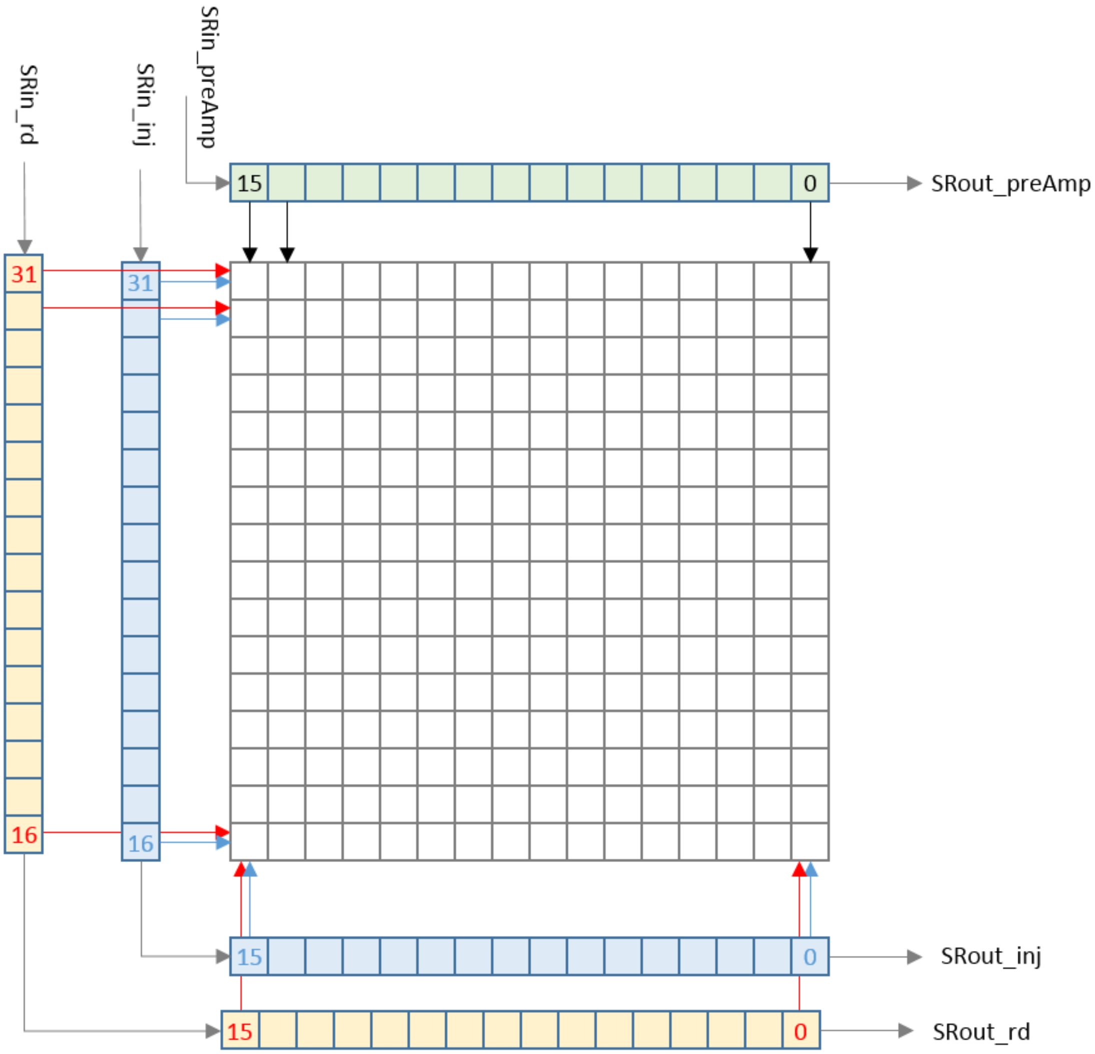

Figure 2: Shift register readout of the pixel matrix. ***SR_preAmp*** *(top) controls what pixel in each of the 16 rows are output to the SF_OUT<15:0> pads.* ***SR_inj*** *and* ***SR_out*** *control which pixels are charge-injected and readout respectively.*

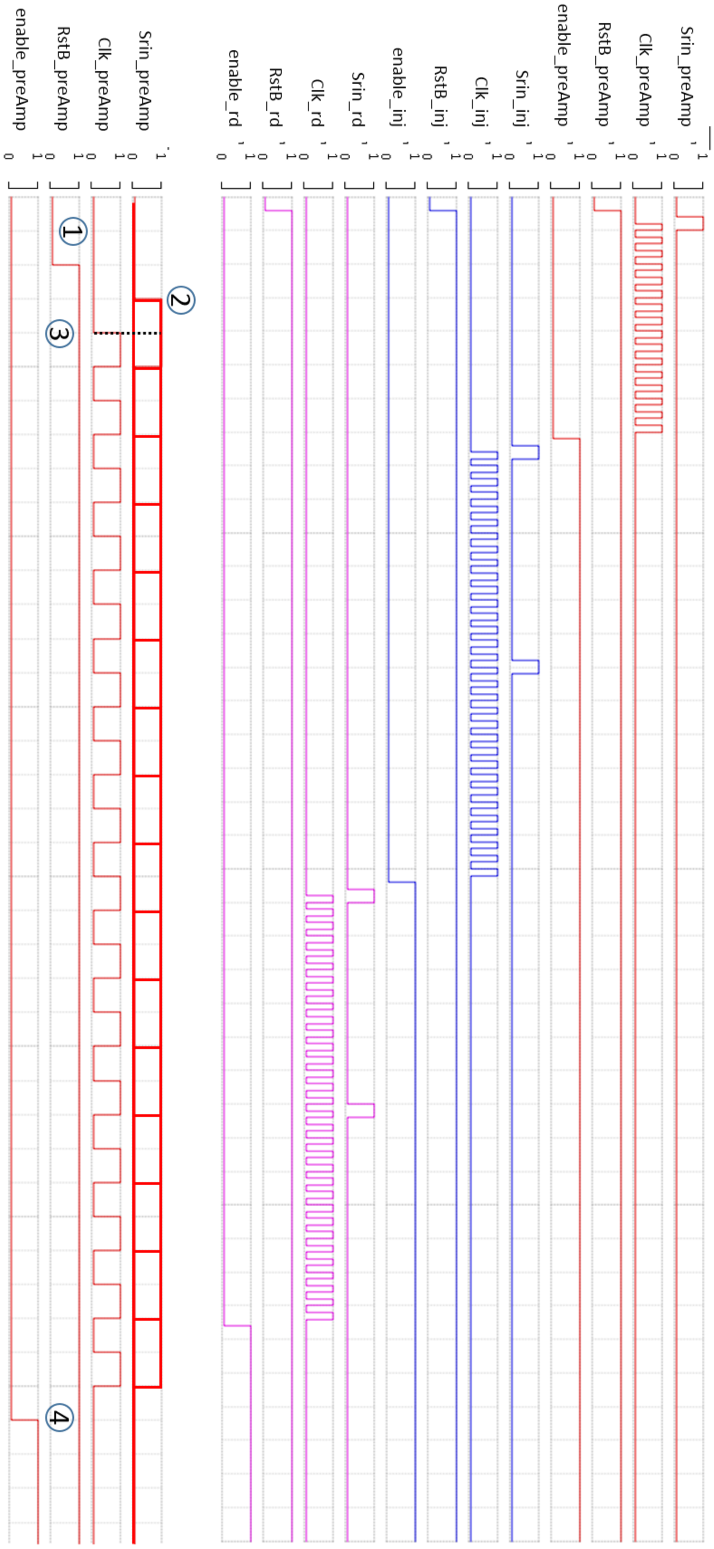

Figure 3: SR load phase: ***SR_preAmp*** *followed by* ***SR_inj*** *followed by* ***SR_rd*** *(top). Bottom: detail of the* ***SR_preAmp****;* **1)** *the initial reset is removed (RstB→ 1);* **2)** *data are presented on SRin and latched on the positive edge of Clk* **(3)** *for 16 times (32 for the longer inj and rd SRs). At the end of the sequence enable goes high* **(4)***.*

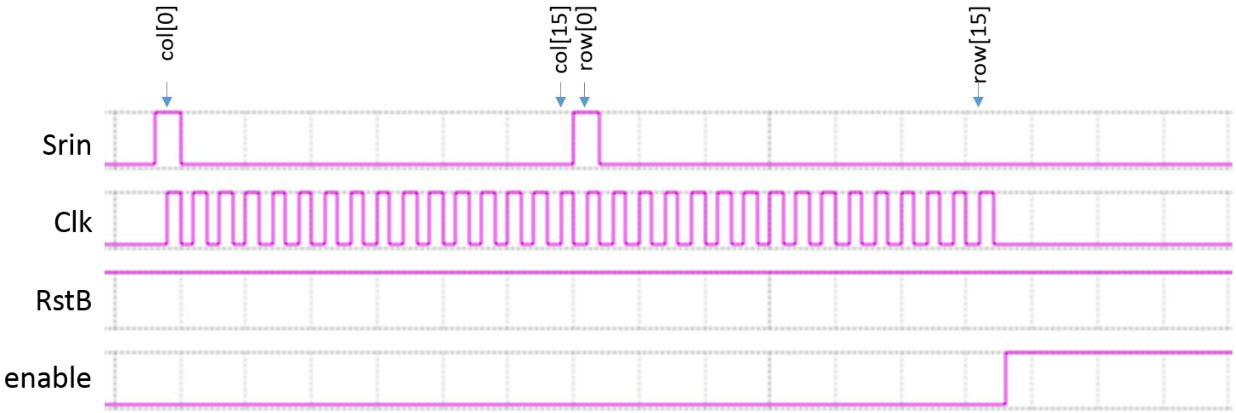

Figure 4: Position of row[15:0] and col[15:0] pixels in the SR load sequence.

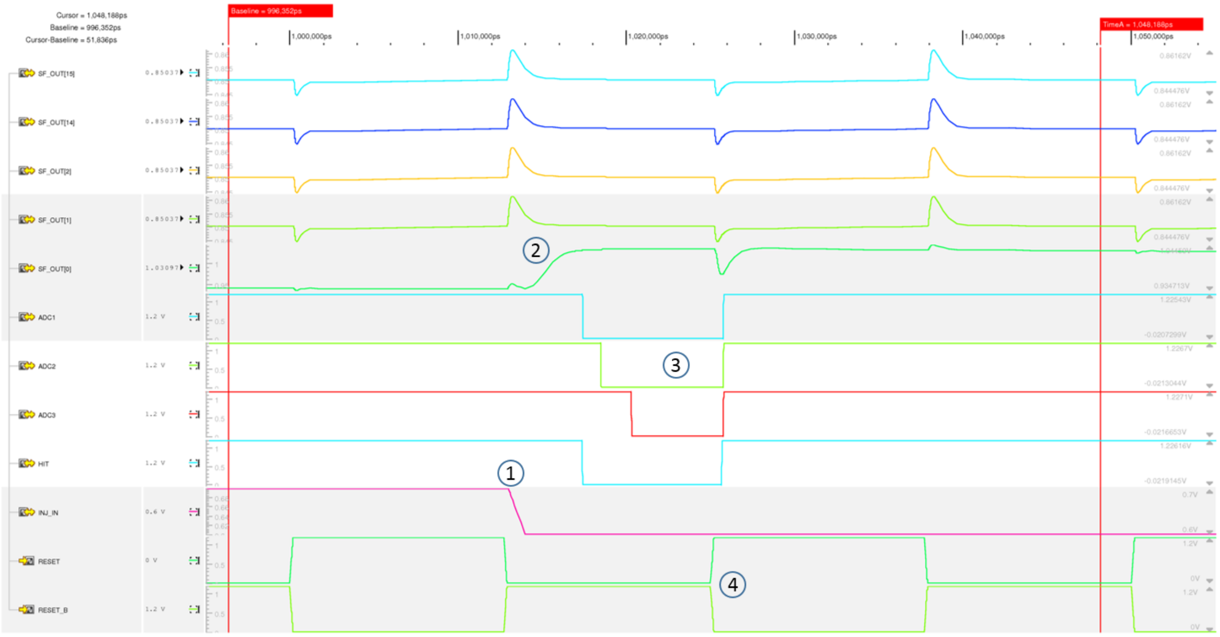

Figure 5: example of readout waveforms. In this case only pixel[0,0] is selected. ***1)*** *charge injection;* ***2)*** *analog signal seen on SF_OUT<0> only;* ***3)*** *digital readout seen on HIT and ADC<1:3>;* ***4)*** *matrix reset. The activity on SF_OUT<15:1> is caused by the reset pulses but can be neglected.*

2.4 Analog readout

Typical operation requires injecting a test signal into a selected pixel(s) and readout the data at the preamplifier output by means of an in-pixel source follower.

To perform such an operation, the pixel has to be enabled for charge injection by means of proper setting of the **SR_inj** (see section 2.1). As an example, injecting charge to the top-left corner pixel, requires to have a logical 1 in SR_inj[31] and SR_inj[15], while keeping all the other SR output cell bits to 0.

The charge injection takes place by providing a negative analog pulse signal at the **INJ_IN** pad. Notice that a 15fF injection capacitance is connected to the preamplifier input. Thus, a 10.6 mV input pulse corresponds to a 1000 electrons input charge.
A 500 ps delay between the edge of the **Reset** (**Reset_B**) signal and the input test pulse should be guaranteed for proper operation.

The analog front-end includes a 35fF MoM capacitor emulating the detector capacitance. This capacitance can be connected or disconnected to the preamplifier input by means of the **CD_EN** input pin, common to the whole matrix. (CD_EN=1.2--> all the capacitance are connected to the preamplifier input).

The preamplifier outputs are fed to the **SF_OUT[15:0]** pads. There is one SF_OUT pad per row, and one column at a time can be selected by properly configuring the **SR_preAmp** (see section 2.1).
As an example, a logical 1 in SR_preAmp[15] allow to readout the preamplifier outputs for all the pixels of the left-most column.
Notice that the preamplifier output is connected to the pad through an in-pixel source follower stage providing a gain G=0.90V/V.

2.4 Disabling of DLL

Since the DLL test structure shares the same power lines of the analog chip (VSS! and TAVDD!), to disable it it is necessary to remove the biasing and inputs as follow:

DLL_ICPbias	Analog Bias	0 V (VSS!)
DLL_Clk	Digital input	0 V (VSS!)
DLL_in	Digital input	0 V (VSS!)
DLL_start	Digital input	0 V (VSS!)
DLL_rstB	Digital input	1.2V (TAVDD!)
DLL_enable	Digital input	0 V (VSS!)
DLL_SRin	Digital input	0 V (VSS!)
DLL_In<8:1>	Digital input	0 V (VSS!)